MBE Growth and Characterization of HgCdTe Heterostructures for Multi-Spectral Infrared Focal Plane Arrays

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Abstract

MBE growth of HgCdTe affords excellent control of film layer thicknesses which are required to achieve a stacked simultaneously integrating two-color focal plane array. For the near term, a hybrid design using back-to-back ion implanted diodes in MBE grown material is being pursued. This structure could have as few as two layers, although three layers are preferred to insure full spectral separation and widen manufacturing tolerance windows. The structure also affords the ability to quantify progress in the growth of materials for monolithic approaches, which are in the more distant future. Progress in the growth of MBE films meeting the needs of this structure is presented.

Introduction

Multi-spectral sensors offer the possibility of improved clutter rejection and improved recognition range. The proper fusing of the information from each spectral band is key to the realization of these advantages. Some fusion techniques, such as signal differencing, require excellent spatial and temporal correlation of the signals from each band. A stacked, co-located pixel architecture capable of simultaneous integration of the spectral bands meets these requirements. One such architecture is the two color, stacked, co-located, three terminal back-to-back diodes pixel.

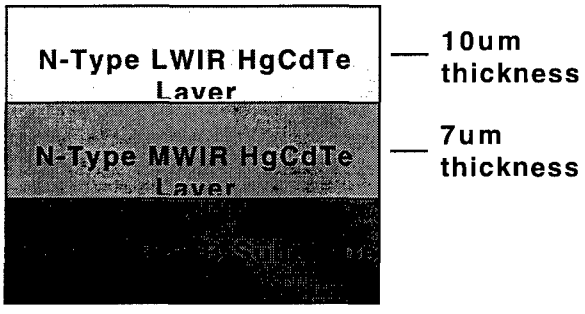
Two color, simultaneous integration HgCdTe back-to-back diodes staring IRFPAs have been produced by both SBRC [1] and Loral [2]. In both cases these are hybrid structures, with the HgCdTe diode array indium bump-bonded to a silicon read-out IC (ROIC). The SBRC approach is a grown N-P-N structure while the Loral approach is a grown P-N-N-P structure. Both approaches require the growth of heterojunctions, which require precise positioning of the P-N junction with respect to the compositional junction. Diode isolation and contacting the middle layer of the back-to-back diodes necessitate the formation of passivated and insulated small, deep holes and trenches with precisely controlled depth. High P-type doping is also required to reduce contact resistance. All of these requirements demand sophisticated, well controlled HgCdTe growth and processing techniques.

Ultimately, a monolithic focal plane array, in which the HgCdTe is grown directly on the silicon ROIC is desirable. Such an array will be the most robust possible. Unfortunately, the HgCdTe structures cannot be grown on top of the individual components of the IC itself. Currently silicon IC technology is incapable of providing the large amounts of bare silicon required for a practical high performance array. In the near future, hybridization is the only method available to demonstrate two-color array technology and capabilities.

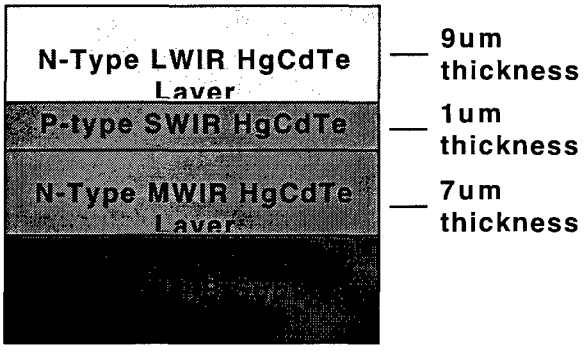
Implanted Diode Two Color Architecture

A new hybrid method of producing stacked, back-to-back HgCdTe diodes for two color detection is proposed. The new architecture, Implanted Diode Two Color (IDTC), utilizes many of the processes and techniques developed at Texas Instruments for VIP™ and HDVIP infrared FPAs. As in the VIP and HDVIP structures, diodes are formed in the IDTC structure by ion implanting indium doped and vacancy doped (or vacancy and Group 1B impurity doped) P-type HgCdTe. The implant process produces a thin N^+ damage layer. Hg interstitials emanating from this layer annihilate vacancies and displace Group 1B dopants (if present), resulting in the formation of a mid to high 10^{14} cm^{-3} indium doped N-type region surrounding the N^+ damage layer. The depth of the junction is controlled by the acceptor concentration and the dose and energy of the implant.

The simplest implementation of the IDTC structure requires only two indium doped N-type layers of HgCdTe grown on a CdZnTe substrate, as shown in Figure 1a. The composition of each layer is chosen to give the desired cutoff wavelength for each spectral band to be detected. After converting the HgCdTe layers to P-type, implanted diodes are formed in each layer to detect the IR radiation absorbed in that layer. The initial spectral bands chosen to demonstrate the IDTC concept will be the MWIR and the LWIR bands. The thickness of the MWIR layer is chosen so that MWIR radiation is totally absorbed by the MWIR layer and a large fraction of the optically generated minority carriers are collected by the MWIR diode. Reasonable thickness control must be maintained for both layers to insure each diode is contained in its respective layer. Extension of a diode into the other layer could result in MWIR diode-to-



a. Simple Implementation



b. Advanced Implementation

Figure 1. Two as grown IDTC HgCdTe structures. Since the preferred growth technique for either structure is MBE, the CdZnTe substrate is shown with a (211)B orientation. The advanced structure provides more process margin and reduced spectral crosstalk.

LWIR diode shorting or severe spectral crosstalk. This problem can be eliminated by the growth of a P-type layer between the MWIR and LWIR layer that is doped with an extrinsic dopant with low diffusivity, such as arsenic. This more advanced structure is shown in Figure 1b. By increasing the bandgap of the arsenic doped layer at least 4kT higher than the bandgap of the MWIR layer, minority carrier confinement in the MWIR layer can be effected, improving spectral crosstalk.

The advanced structure is a still a relatively simple structure to grow since the SWIR layer requires only moderate P-type doping and p-n junction quality is not important unless the LWIR diode junction extends to the SWIR layer. Excellent thickness control and the low temperature in-situ growth of layers of different composition and doping of HgCdTe make MBE the preferred growth technique for this structure.

A cross-section of the IDTC pixel utilizing the advanced three layer HgCdTe film is shown in Figure 2. The resulting back-to-back diodes pixel is an N-P-N structure. The process sequence to produce this structure is as follows:

1. MBE growth of 3 HgCdTe layers on a CdZnTe substrate
2. Trench etched (diode isolation)
3. CdTe/ZnS passivation deposited and annealed under Te-rich conditions to convert N-type layers to P-type
4. Small ohmic contact made to LWIR P-type layer
5. LWIR diode formed by selective implantation
6. LWIR diode contact formed
7. Insulation layer deposited, patterned, and etched
8. Bumps contacting the LWIR diode and the LWIR P-type layer formed
9. HgCdTe detector arrays sawed apart, hybridized to silicon ROICs, and epoxy inserted between the

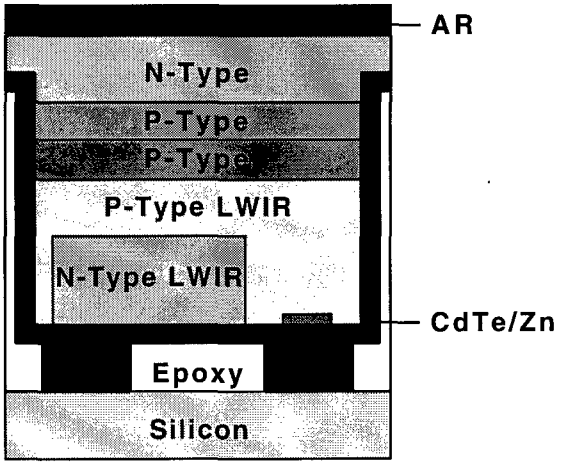


Figure 2. Cross-section of the Implanted Diode Two Color (IDTC) architecture.

HgCdTe array and ROIC
10. CdZnTe substrate selectively removed
11. MWIR diode formed by blanket implant
12. Anti-reflective coating and passivation deposited
13. Bond pads on silicon ROIC etched and arrays sawed apart

Processes that are the same in VIP and IDTC array fabrication include HgCdTe doping, HgCdTe surface passivation, diode formation, diode ohmic contact formation, insulation deposition, and insulation via hole etching. The IDTC process also utilizes HDVIP processes to make small (<5 μm diameter) ohmic contacts to the P-type LWIR layer and to selectively remove the CdZnTe substrate from HgCdTe epi-layers.

The commonality of many processes in the fabrication of IDTC and VIP arrays is a distinct advantage of the IDTC architecture at Texas Instruments. But the IDTC architecture has other advantages over the grown junction back-to-back diodes architectures:

1. Simple MBE growth technology requiring no grown junctions and no P^+ layer
2. LWIR diode junction (the most difficult junction to passivate) not on trench side wall (the most difficult surface to passivate)
3. No deep, passivated, insulated via holes crossing a p-n junction to form
4. Better fill factor since no hole through HgCdTe to contact middle layer required

The development of a dry etched trench, trench side wall passivation, and trench isolated MWIR diode formation has just begun. These processes are all dependent upon formation of a low damage, deep, narrow trench of well controlled depth. A result of the first trench etching experiments is shown in Figure 3. Trenches 13 μm deep and 7.5 μm wide were obtained using a combination ion milling/wet etching process. The trench depth is near optimum for the IDTC structure. Trench width needs to be reduced for future small pixel arrays, but present width is deemed adequate for 40 μm or larger pitch pixels.

MBE Growth and Characterization

MBE film growth has begun in an effort to achieve the structures shown in Figure 1. Two types of films are being grown: (1) Single layer films, both MWIR and LWIR, and (2) Triple layer structures consisting

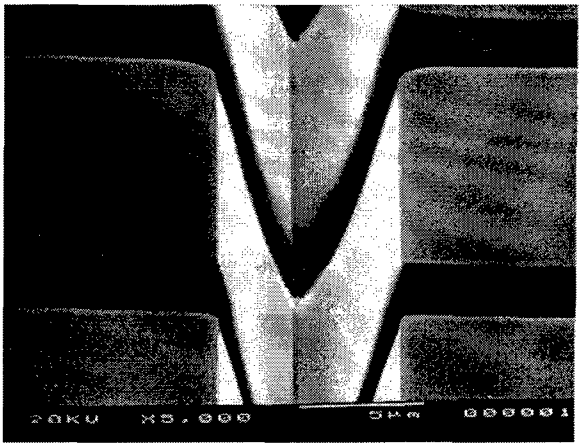


Figure 3. Trenches etched in HgCdTe by an ion milling/wet etching technique. The trenches are 13 μm deep and 7.5 μm wide at the top.

of an LWIR surrounded on both surfaces by MWIR layers. This latter structure is aimed at simplifying device characterization - the two MWIR layers act as surface passivation for the ion implanted junctions formed in the LWIR layer.

The requirements to be met for these structures, at least for the LWIR layer, is a cutoff in the 10 μm range, corresponding to an x-value (cadmium mole fraction) of approximately 0.22, an n-type carrier concentration less than $3x10^{15}$ cn^{-3}, an electron mobility greater than $8x10^4$ cm^2/V-sec, and a dislocation density (as measured by the etch pit density, or EPD) less than $3x10^5$ cm^{-2}. The last requirement is necessary to achieve satisfactory 1/f noise behavior.

Some results obtained so far on this program are

Table 1. Properties of MBE films

Run ID	x Value	Thick μm	EPD cm-2	n cm-3	Mobility cm2/V-sec	Lifetime nsec
195	0.287	4.24	poly	p 7.47E16	268	
196-1	~.28	4.17				
196-2	0.239	5.22	2.00E+06	2.22E+15	62,800	507
207-1	~.28	1.31				
207-2	0.223	5.37	2.00E+06	3.47E+15	78,200	650
208-1	~.28	1.33				
208-2	0.236	5.26	2.30E+06	3.88E+15	60,800	1170
209-1	~.28	1.38				
209-2	0.222	5.47	e7	2.44E+15	56,600	348
219	0.225	5.99	1.20E+06	1.40E+15	92,300	1250
220	0.235	5.66	2.60E+06	1.27E+15	75,500	1440
221	0.228	5.89	2.40E+06	2.47E+15	75,400	1110
222	0.22	5.99	7.20E+05	2.04E+15	117,000	640
223	0.227	5.64	8.50E+05	?		680
228-1	~.28	2.18				
228-2	0.214	6.56	2.40E+05	1.57E+15	106,000	960
236	0.225	8.38	4.50E+05	1.60E+15	93,400	
240	0.302	8.37	1.10E+06	1.31E+15	34,000	

shown in Table 1. In particular, the properties of run 228-2 are very close to that which is required for the

LWIR layer. Future work is aimed at improving the quality of the MBE layers versus the required specification. Diodes are also to be fabricated in MBE films and characterized as to their performance as IR detectors. Past work indicates that diodes fabricated on material with properties similar to those of run 228-2 should yield very satisfactory IR photodetectors.

References

[1] P. Love, et. al., "128x128 Simultaneous-Integration Two-Color HgCdTe FPAs", Proceedings of the IRIS Detectors Specialty Group Symposium, August 16-17, 1995, p. 169-186.

[2] A. Hairston, et. al., "Simultaneous MW/LW Dual-Band MOCVD HgCdTe IRFPAs", IRIS Detectors Specialty Group Symposium, July 31-August 1, 1996, NIST, Boulder, CO.

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